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Substitute for Form PTO-1449

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 3

Complete if known

Application Number	09/880,333
Filing Date	June 13, 2001
First Named Inventor	Francois Silve
Group Art Unit	Not yet assigned
Examiner Name	Not yet assigned
Attorney Docket Number	21891.04000

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant Of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
T.P.	A1	3,617,714		Kernighan et al.	11/02/1971	
T.P.	A2	4,593,363		Burstein et al.	06/03/1986	
T.P.	A3	4,612,618		Pryor et al.	09/16/1986	
T.P.	A4	4,630,219		DiGiacomo et al.	12/16/1986	
T.P.	A5	4,924,430		Zasio et al.	05/08/1990	
T.P.	A6	5,053,980		Kanazawa	10/01/1991	
T.P.	A7	5,095,454		Huang	03/10/1992	
T.P.	A8	5,111,413		Lazansky et al.	05/05/1992	
T.P.	A9	5,144,563		Date et al.	09/01/1992	
T.P.	A10	5,187,784		Rowson	02/16/1993	
T.P.	A11	5,197,015		Hartoog et al.	03/23/1993	

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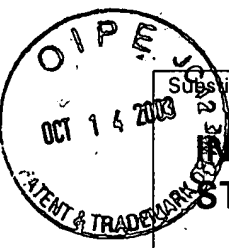
OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ⁴
T.P.	C1	Venkatesh, S.V. (1995) "Hierarchical Timing-driven Floorplanning and Place and Route Using a Timing Budgeter," <i>IEEE 1995 Custom Integrated Circuits Conference</i> pp.469-472	
T.P.	C2	Frankle, Jon (1992) "Iterative and Adaptive Slack Allocation for Performance-driven Layout and FPGA Routing," <i>29th ACM/IEEE Design Automation Conference</i> pp. 536-542	
T.P.	C3	Ikeda, Toshio et al. (1992) "aTAPLAS3: A Constraint Driven and High-performance Layout System for Huge Design," <i>IEEE 1992 Custom Integrated Circuits Conference</i> pp. 28.5.1 - 28.5.4	
T.P.	C4	Hitchcock, Robert B. et al. (1982) "Timing Analysis of Computer Hardware," <i>IBM J. Res. Develop.</i> 26(1):100-105	

Examiner Signature	<i>Maupham</i>	Date Considered	12/03
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T.P.	A12	5,218,551		Agrawal et al.	06/08/1993	
T.P.	A13	5,224,056		Chene et al.	06/29/1993	
T.P.	A14	5,237,514		Curtin	08/17/1993	
T.P.	A15	5,239,493		Sherman	08/24/1993	
T.P.	A16	5,251,197		Leube et al.	10/05/1993	
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T.P.	A18	5,461,576		Tsay et al.	10/24/1995	
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T.P.	A20	5,483,461		Lee et al.	01/09/1996	
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T.P.	A22	5,778,216		Venkatesh	07/07/1998	

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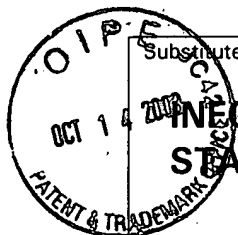
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T.P.	C5	Hauge, Peter S. et al. (1987) "Circuit Placement for Predictable Performance," <i>IEEE International Conference on Computer-Aided Design</i> pp. 88-91		
T.P.	C6	Garbers, J. et al. (1990) "VLSI-Placement on Routing and Timing Information," <i>EDAC Proceedings of the European Design Automation Conference</i> pp.317-321		
T.P.	C7	Shragowitz, E. et al. (1988) "Predictive Tools in VLSI System Design: Timing Aspects," <i>CompEuro 88 – System Design: Concepts, Methods and Tools</i> pp.48-55		
T.P.	C8	Sutanthavibul, S. et al. (1991) "Dynamic Prediction of Critical Paths and Nets for Constructive Timing-Driven Placement," <i>28th ACM/IEEE Design Automation Conference</i> pp. 632-635		
T.P.	C9	Kernighan, B.W. et al. (1970) "An Efficient Heuristic Procedure for Partitioning Graphs," <i>The Bell System Technical Journal</i> pp.291-307		

Examiner Signature	<i>Mauphan</i>	Date Considered	12/03
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T.P.	C10	Quinn, Jr., et al. (1979) "A Forced Directed Component Placement Procedure for Printed Circuit Boards," <i>IEEE Transactions on Circuits and Systems</i> CAS-26(6):377-388	
T.P.	C11	Teig, Steven et al. (1986) "Timing-Driven Layout of Cell-Based lcs," <i>VLSI System Design</i> VII(5):63-73	
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T.P.	C13	Sarrfzadeh, M. et al. (1997) "A Delay Budgeting Algorithm Ensuring Maximum Flexibility in Placement," <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> 16(11):1332-1341	
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